INTEGRATED CIRCUIT MEMORY DEVICES AND OPERATING METHODS THAT ARE CONFIGURED TO OUTPUT DATA BITS AT A LOWER RATE IN A TEST MODE OF OPERATION

Abstract

Integrated circuit memory devices include a memory cell array that is configured to output data bits in parallel at a first data rate. An output circuit is configured to serially output the data bits to an external terminal at the first data rate in a normal mode of operation, and to serially output the data bits to the external terminal at a second data rate that is lower than the first data rate in a test mode of operation. Accordingly, the memory cell array can operate at a first data rate while allowing the output circuit to output data to an external terminal at a second data rate that is lower than the first data rate, in a test mode of operation.